

# Facilitating Testability of TLM FIFO: SystemC Implementations

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## Abstract

*TLM is a high-level approach to modeling digital systems with an emphasis on separating computations from communications within a system. With the evolution of design methodologies to transaction level the need for definition of DFT (Design for Test) techniques at this very high level of abstraction arises. This paper focuses on the implementation of three different high-level testing strategies for TLM FIFO as the basic TLM communication channel. These strategies are implemented by adding Built-in Functional Self Test (BIFST) utilities to the channels and computation units. We present SystemC implementations of the utilities that we have developed in the form of new SystemC classes and methods.*

## 1. Introduction

With the increasing complexity of digital systems, and shrinking time to market, Electronic System Level (ESL) design has emerged as the main design methodology for implementing large digital systems. The evolution of ESL design methodologies has introduced *Transaction Level Modeling (TLM)*. TLM is a transaction-based modeling approach, originally based on high-level programming languages such as C++ and SystemC, which emphasizes on separating communication from computation within a system. In the TLM notion, communication mechanisms are modeled as abstract channels accessed resorting to interface functions [1].

Contrary to the migration of design methodologies from gate and register transfer levels to higher abstraction levels such as TLM, testing and testability techniques are still mostly performed at lower abstraction levels. It is thus gaining importance for system level designers the introduction of DFT techniques to insert testability features directly at TLM level in a completely automatic way, without

concerning themselves with the intricacies of lower level implementations.

In [2] we introduced a testing methodology applicable at the TLM level during the system level design phase. We proposed our test techniques that can be applied to the design even before hardware/software partitioning, and we focused on TLM communication channels. In the present paper we present the SystemC implementations of different TLM Testing Strategies introduced in [2].

The paper is organized as follows: Section 2 has an overview on the TLM Testing Methodology presented in [2]. Section 3 provides the SystemC Implementation for three proposed TLM testing strategies, and finally Section 4 concludes the paper.

## 2. TLM Testing Methodology

This section presents an overview of the proposed high-level TLM testing methodology proposed in [2].

In [2] we took the preliminary steps toward definition of DFT at TLM abstraction level by developing a testing methodology during the system level design phase, before hardware/software partitioning with a focus on TLM communication channels. Since the only possible and reasonable testing strategy at a very high abstraction level like TLM is functional testing, we provided a design methodology capable of defining functional tests at TLM abstraction level, to be later on automatically translated into Built-in Functional Self Test (BIFST) facilities in the final product. These BIFST facilities are added into each computation unit and the communication channel in the TLM design and can be later synthesized either into hardware or software according to the designer's choices and needs. Figure 1 shows the proposed test architecture of [2] in which each of the computation units (Writer and Reader) and the communication channel are modified to include the required BIFST facilities.

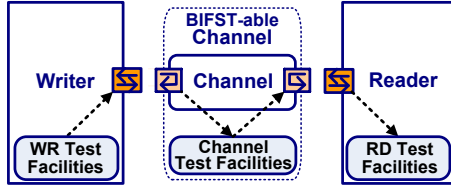


Figure 1 TLM Test Architecture [2]

Three different testing strategies are considered in this architecture. These are: Transaction Testing, Self Testing, and Integration Testing. Each of these testing strategies can be implemented by definition of the involved blocks in test procedure and implementing the required facilities in them. The BIFST units added inside computation units and the communication channels include Test Data Generators (TDGs), Test Response Evaluators (TREs), Test Controllers, and Interfaces [2].

The proposed architecture is a general architecture for implementing different testing strategies and a designer can have his/her own test approach and implementations for the added facilities. In the next section we present the SystemC implementations of BIFST facilities and the TLM definition of BIFST-able *tlm\_fifo*, as the most basic TLM primitive channel in TLM Library, based on the FSM model test approach presented in [2] and [3].

### 3. SystemC Implementations

In the test architecture of Figure 1 the implementation of TDG and TRE units correspond to the definition of both test cases and test oracles for all the TLM methods of the communication channel under test. Test Oracles are the set of operations needed to check the correct execution of test cases. These operations include the comparisons to check the state of the channel and values returned to outside, as well as methods to be performed during the test procedure in order to put the channel in the required working states and prepare it for test execution [3].

Our overall idea is to define, for each method of *tlm\_fifo* primitive channel, based on its FSM model, a suitable functional test sequence. In particular, we generate the test cases for each *tlm\_fifo* method by trying to stress it in different operational states, satisfying the transition coverage criterion [3]. Table 1 shows the test sequences for three methods of FIFO (*put()*, *nb\_put()*, and *nb\_can\_put()*) implementing WRITE functionalities. Test cases for all other methods of *tlm\_fifo* have been generated in a similar way.

The SystemC implementation of these test sequences will be different according to the chosen

testing strategy. In the following subsections we see SystemC implementations of the proposed BIFST facilities for three different strategies introduced in Section 2.

Table 1 - Test Sequences for *tlm\_fifo* Methods (Write Functionalities)

#	<i>put()</i>	#	<i>nb_put()</i>	#	<i>nb_can_put()</i>
1	✓ <i>put()</i>	1	<i>nb_put()</i>	1	<i>nb_can_put()</i>
<i>n-1</i>	✓ <i>put()</i>	<i>n-1</i>	<i>nb_put()</i>	1	<i>put()</i>
1	✓ <i>put()</i>	1	<i>nb_put()</i>	1	<i>nb_can_put()</i>
1	<i>get()</i>	1	<i>get()</i>	<i>n-1</i>	<i>put()</i>
1	<i>get()</i>	<i>n-2</i>	<i>get()</i>	1	<i>nb_can_put()</i>
<i>n-2</i>	<i>get()</i>	1	<i>get()</i>	<i>n+1</i>	<i>get()</i>
1	<i>get()</i>	1	<i>get()</i>	1	<i>nb_can_put()</i>
1	<i>get()</i>	1	<i>nb_put()</i>	1	<i>put()</i>
1	✓ <i>put()</i>	1	<i>peek()</i>	1	<i>peek()</i>
1	<i>peek()</i>	1	<i>nb_put()</i>	1	<i>nb_can_put()</i>
1	✓ <i>put()</i>	1	<i>get()</i>	1	<i>put()</i>
1	<i>get()</i>	1	<i>get()</i>	1	<i>get()</i>

#### 3.1. Transaction Testing Implementation

Transaction testing strategy includes testing the transactions between channel and computation units independently. This can be done by testing Write Transactions or Read Transactions by checking the correct functionality of the interconnection between the Writer/Reader and Channel without using the other side Reader/Writer. Figure 2.a and b show the implementation of Write and Read Transaction tests in the architecture of Figure 1.

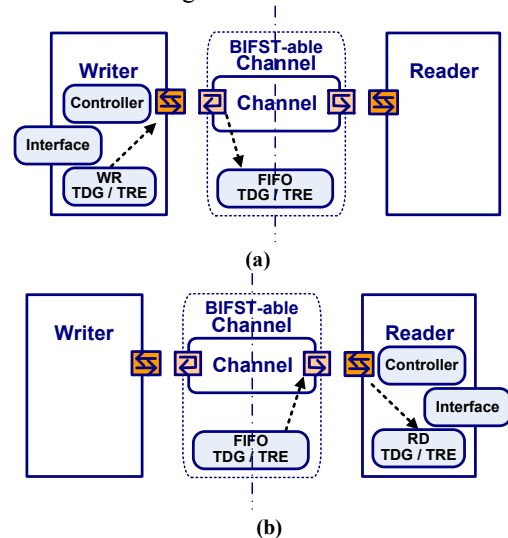


Figure 2 Transaction Testing:  
(a) Write Transaction (b) Read Transaction

This strategy has several advantages. First of all the “writing” and “reading” functionalities of the channel can be easily tested autonomously (e.g., testing

the writing functionalities does not require the reader to be involved). The reader and writer are not concurrently involved in the test, and their related activities do not need any ad-hoc timing. Each of them has the responsibility of testing the methods of the channel actually used. The main drawback of this approach is that the communication channel and the computation units have to be modified to include the test facilities which lead to an overhead.

In this test strategy, each single block receives external requests concerning the beginning of the test phase. Then the corresponding computation unit (Writer/Reader) waits until the communication channel becomes ready for performing test. After this, the Transaction Test mode is activated for the communication channel and the test sequence starts by applying generated test cases into the channel. Since only the Writer/Reader and that part of the channel that is responsible for Writing/Reading are participating in performing a Transaction test, the communication channel should emulate the other side's functionality by calling the methods internally. For example the *put()* functions check-marked in the first column of Table 1 are test transactions issued by the Writer. But the *get()* and *peek()*s should be emulated inside the FIFO. As shown in Figure 2, for testing Write Transactions the TRE unit of channel performs test oracles by responding to the test transactions issued by the Writer; and for testing Read functionalities the TDG unit of Reader generates test cases, TRE<sub>Reader</sub> plays the role of Test response evaluator, and TRE<sub>FIFO</sub> performs operations for moving FIFO between the required working states.

The generated test cases and Oracles are added into SystemC description of Writer, Reader and the Channel. We implement the new SystemC class of *testable\_tlm\_fifo* which inherits from *tlm\_fifo* and overrides all the FIFO methods to include BIFST facilities inside [2]. The functions which are going to be emulated internally by FIFO are defined as new TLM methods in the new BIFST-able version of *tlm\_fifo*. These methods are started with “t\_” indicating the “Test” version of each method and include: *t\_nb\_peek()*, *t\_compare()*, *t\_get()*, *t\_put()*, and *t\_peek()*. The first two functions are used in the implementation of comparison oracles for checking the values and states. The *t\_nb\_peek()* method is a non-blocking test method which always *nb\_peek()* the most recently written element to the FIFO. Its difference with *nb\_peek()* is that it is called internally from the FIFO and reads the most recently element instead of the first one. The *t\_compare()* method is for comparing the test response (value and state of FIFO) with the fault-free

reference model of FIFO. The *t\_get()*, *t\_peek()*, and *t\_put()* methods are implemented by calling the original *get()*, *peek()* and *put()* methods [2], respectively.

```

//put()
template <typename T>
inline
void
testable_tlm_fifo<T>::put(const T& val)
{
00 //Test Mode
01 if (m_N Tmode == true){
02 //Full: Unblock Writer Thread
03 if (!tlm_fifo<T>::nb_can_put())
04     fifo_full_event.notify(
                                SC_ZERO_TIME);
05 }
06 //Normal Operation
07 tlm_fifo<T>::put(val_);
08 wait(0, SC_NS);
09 //Test Mode
10 if (m_N Tmode == true){
11 //Before FIFO becomes Full
12 if (m_test_num <= m_size)
13 {
14     in >> TestData;
15     t_compare(t_nb_peek(), TestData);
16     m_test_num++;
17 }
18 //Before FIFO becomes Empty
19 else if (m_test_num == m_size+1)
20 {
21 //Peek and Compare the MRW
22 in >> TestData;
23 t_compare(t_nb_peek(), TestData);

24 //Get until FIFO Empty
25 while(tlm_fifo<T>::nb_can_get())
26 {
27     x = t_get();
28 }
29 //EMPTY: Unblock Reader Thread
30 fifo_empty_event.notify(
                                SC_ZERO_TIME);
31 wait(1, SC_NS);
32 }
33 //FIFO is Empty
34 else if (m_test_num == m_size+2)
35 {
36     in >> TestData;
37     t_compare(x, TestData);
38 //Back to Unblock Reader Thread
39 wait(1, SC_NS);
40 }
41 else if (m_test_num == m_size+3)
42 {
43     in >> TestData;
44     t_compare(x, TestData);
45     x = t_get();
46 }
47 } }

```

Figure 3 SystemC Description of Overridden *put()* Method in *testable\_tlm\_fifo*

The class definition of *testable\_tlm\_fifo* including the header of the new overridden methods, threads, new test methods, and data types is presented in [2]. In Figure 3 the SystemC descriptions for overriding the

*put()* method as an example of implementing the test sequence of Table 1 is shown. The Writer issues the test transactions to the FIFO by calling this overridden *put()* method and FIFO responds to them by running the function of Figure 3. The deterministic test data are fed from an input file which is shared between TDG and TRE units (e.g. *in >> TestData* in Line 14). The *m\_N\_Tmode* (Lines 1 and 10) indicates the Test mode and the *m\_test\_num* variable is for counting the steps of the test sequence. Two threads, called *unblock\_writer* and *unblock\_reader*, are defined for *testable\_tlm\_fifo* to provide parallelism to FIFO [2]. They enable continuing the sequence of actions when the FIFO is blocked to perform a blocking TLM function and cannot continue the sequential code of its *put()* method. These threads are activated by notifying their corresponding events from *put()* method (Lines 4, 30, 39).

### 3.2. Channel Self-Testing Implementation

Channel Self-Testing Strategy tests a channel as an isolated component, without consideration of its connection to the Writer and Reader. In this strategy only the FIFO needs to be modified. The reader and writer are not involved in the test and do not have any information about the topology of the system. The drawback of this approach is the overhead of modifying the communication channel to include the proposed BIFST facilities.

The implementation of this strategy is done by the definition of TDG and TRE units and the test controller inside *tlm\_fifo*. A new *SC\_THREAD* called *t\_self\_test* is described inside the *testable\_tlm\_fifo* SystemC description and is initiated by activating the Self Test mode from outside the FIFO. This thread performs the test sequences for each method of *tlm\_fifo*. The *tlm\_fifo* methods generated in test sequences of Table 1 are replaced by their “*t\_*” versions and are called internally with the same ordering inside the FIFO.

### 3.3. Integration Testing Implementation

The last strategy is for testing the integration between Writer, FIFO and Reader. In the Integration Testing strategy, FIFO always runs in its normal mode and is not involved in the test procedure. The reader and writer are concurrently responsible for performing tests by some external synchronization and timing considerations. Both the reader and writer should be aware of the topology of the communication channel to which they are connected and need a protocol for being synchronized with each other.

This strategy is implemented by definition of  $TDG_{Writer}$  and  $TRE_{Reader}$  units for testing Write

functionalities and  $TDG_{Reader}$  and  $TRE_{Writer}$  units for Read methods. Also we need to define the synchronization protocol and the test controller.

The generated test cases and test oracles are added into the SystemC description of Writer and Reader and the test control is implemented by using *ok\_to\_put()*, *ok\_to\_get()*, *ok\_to\_peek()* methods of FIFO and *wait()* statements which enable the synchronization between Writer and Reader. Figure 4 shows part of a SystemC code implementing the  $TRE_{Reader}$  and Reader Controller for the *put()* method test procedure. Before performing any response, the Reader waits for FIFO to complete the execution of *put()* transaction issued by the Writer. This is done by using *ok\_to\_get()/ok\_to\_peek()* methods which notify an event whenever a write is done inside the FIFO. In other words, the SystemC codes of the body of the overridden methods in Transaction Testing implementation, here in Integration Testing are used as portions of codes between *wait(ok\_to\_get())/wait(ok\_to\_peek())*s. The implementation of the other side unit ( $TDG_{Writer}$ ) is the same as Transaction Testing strategy and consists of a sequence of *put()* invocations.

```

//Reader TRE
. . .
while (nb_can_put()){
    wait(ok_to_peek());
    nb_peek(val_, m_num_readable-1);
    tr_compare(val_, TestData[i]);
    wait(SC_ZERO_TIME, NS);
}
. . .

```

Figure 4 SystemC Description for TRE in Write Transaction Test Strategy

## 4. Conclusions

In this paper we focused on SystemC implementations of *testable\_tlm\_fifo* for three different TLM Testing Strategies introduced in [2]. The proposed SystemC implementations can be used as DFT rules in the process of TLM design.

## 5. References

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- [2] H. Alemzadeh, S. D. Carlo, F. Refan, P. Prinetto, Z. Navabi, “Plug & Test at System Level via Testable TLM Primitives,” To appear in Proc. of *International Test Conference (ITC'08)*, Pre-prints Available at: <http://orion.polito.it/~dicarlo/plist/ITC08.pdf>
- [3] H. Alemzadeh, S. D. Carlo, A. Scionti, P. Prinetto, Z. Navabi, “Functional Testing Approaches for “BIFST-able” *tlm\_fifo*,” To appear in Proc. of *IEEE International High-Level Design Validation and Test Workshop 2008*.